Implementation and Algorithms for the FPD DSM Tree: High-Tower Version

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Description: The first layer of DSM boards places three thresholds on each single PMT. These thresholds are SIZEORDERED th0 < th1 < th2. The thresholds are the same for all PMTs. A register selects which of the three thresholds is used to trigger STAR, if any of the PMTs is above it. The three thresholds are coded into two bits individually for each module and these 8*2 bits are available in the scaler boards. Find a drawing of the FPD-DSM tree at
http://www.star.bnl.gov/STAR/html/fpdl/fy03/electronics/index.html

1. FPD-layer0, FPD-FE/W-001, 002, 003, 005, 006, 007, 008, 009, 010, 011

This Algorithm places thresholds on all 16 8bit input channels. Unused channels need to be zeroed out in the LUTs. These thresholds are size ordered th0 < th1 < th2. An 'or' is build for each threshold, from all the PMTs in each board. The tree threshold bits are propagated to the next layer. This DSM algorithm also contains the HALT-COUNTER mechanics.

Input: up to 16x8bit ADC values

Registers: R0: FPD-PMT-th0 (8)
R1: FPD-PMT-th1 (8)
R2: FPD-PMT-th2 (8)
R3-R12 dummies
R13-15 Halt counter mechanics

LUT: Pedestal subtraction / masking unused channels

1st Clock: Place three thresholds on each 8bit ADC channel

2nd Clock: Combine all channels into one bit per threshold. Bit is set ('1') if any PMT is above the specific threshold

Output: (0-2) threshold-bits
(3-15) empty

2. FPD-layer0, FPD-FE/W-004

Same functionality as FP001. This is the split module. Only the channels 0-6 and 7-13 are used.

Input: 2x7 8bit ADC values; split module
Assignment of North and South is swapped for East and West crate

Ch0-6 East-North; West-South
Ch7-13 East-South; West-North

Registers: R0-R2 same as FP001, no halt counter.

LUT: same as FP001

1st. Clock: same as FP001

2nd Clock: same as FP001

Output: (2 cables)
Lower bits East-North; West-South; ch0-6
(0-2) threshold-bits
(3-15) empty
Upper bits East-South; West-North, ch7-13
(16-18) threshold-bits 0-2
(19-31) empty

3. FPD-layer1, FPD-FE/W-101, North-South modules

Combine 8x 3bits to the high-tube threshold bits of a detector module.

Input: 8x3 threshold bits
Ch0-3 E-N/W-S
Ch4-7 E-S/W-N

Registers: None

LUT: 1:1

1st. Clock: Combine Bits

2nd Clock: Delay

Output: (2 cables)
Lower bits East-North; West-South
(0-2) Threshold Bits
(3-15) empty
Upper bits East-South; West-South
(16-18) Threshold Bits
(19-31) empty

4. FPD-layer1, FPD-FE/W-102, Top/Bottom

Same functionality as FP101; only the first 4 channels are used from the top/bottom modules.

Input: 4*3 threshold bits
Ch0-1 Top
Ch2-3 Bottom

Registers: None

LUT: 1:1

1st. Clock: Combine Bits

2nd Clock: Delay

Output (2 cables)
Lower bits Top
(0-2) Threshold Bits
(3-15) empty
Upper bits Bottom
(16-18) Threshold Bits
(19-31) empty

5. FPD-layer2, L1-FP201

Code the three threshold bits into two bit numbers for the use in the scaler boards. A register selects which threshold is used to trigger STAR.

Input: One Set of threshold bits per detector module
ch0: East-North
ch1: East-South
ch2: East-Top
ch3: East-Bottom
ch4: West-South
ch5: West-North
ch6: West-Top
ch7: West-Bottom

Registers: **L1: index: 0x1e**
The registers R0-R2 are left for compatibility. They do not have any effect in the high-tower version.
R0: ADC-threshold-0 (unused)
R1: ADC-threshold-1 (unused)
R2: ADC-threshold-2 (unused)
R3: FPD-trigger-threshold-select: ’0’-th0; ’1’-th1; ’2’-th2; ’3’-off
R4: FPD Mask (8) 0-off, 1-on
Mask 7-0 is 7=BW, TW, SW, NW, BE, TE, SE, 0=NE
Mask 0x0f is East only, 0xf0 is West only

LUT: 1:1

1st. Clock: Apply mask

2nd Clock: Code threshold comparison into scaler bits separately for all 8 modules.
Two bits per module: ’00’-ADC<th0, ’01’-ADC>th0, ’10’-ADC>th1, ’11’-

ADC>th2. STAR FPD trigger fires, for East and West separately, if any module is above threshold as selected by R3.

Output: **THIS IS WHATS AVAILABLE IN THE LAST DSM**

(0) FPD-trigger East
(1) FPD-trigger West
(2-15) empty

Scalers

(0-1) Threshold Bits – East/North
(2-3) Threshold Bits – East/South
(4-5) Threshold Bits – East/Top
(6-7) Threshold Bits – East/Bottom
(8-9) Threshold Bits – West/South
(10-11) Threshold Bits – West/North
(12-13) Threshold Bits – West/Top
(14-15) Threshold Bits – West/Bottom